

CLAIMS

Sub A² → 1. A data-network comprising:

at least one crossbar, wherein each crossbar comprises N ports;

5 a plurality N of devices each associated with and connected to one port
of one of said crossbars;

wherein each one port of one crossbar comprises:

an input buffer for receiving messages from the device
connected to its port and for sending said messages to the N-1 other
10 ports of said one crossbar;

a plurality N-1 of port output buffers, each corresponding to one
of said N-1 other ports, wherein each port output buffer receives said
messages only from said input buffer of its associated other port;

15 a plurality N-1 of fullness sensors, each associated with one
port output buffer, for measuring the fullness state of its associated port
output buffer;

shutoff means, connected to the fullness sensors associated
with the port output buffers corresponding to said one port at said N-1
other ports, for, when said fullness state for one of said other ports is
20 generally full, indicating to said device connected to said one port not to
send data for the port which is now generally full.

2. A network according to claim 1 wherein each device additionally
comprises N-1 device output buffers, one per the N-1 other ports of said
crossbar.

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3. A network according to claim 2 and wherein each device also comprises a multiplicity of direct memory access (DMA) units for removing data from at least one of said device output buffers.

4. A network according to claim 1 and wherein each crossbar comprises an arbiter for providing said messages from said N-1 port output buffers to said device connected to its port only if said device is not full.

Sub A³ → 5. A network according to any of the preceding claims, and wherein each port comprises a bus link connected to said corresponding associated device.

10 6. A switch for a data network, the data network including at least one crossbar having N ports and the switch being connectable to one of said N ports, the switch comprising:

a multiplicity of switch output buffers, one per the N-1 other ports of said crossbar; and

15 at least two direct memory access (DMA) units, each associated with at least one of said switch output buffers, for removing data from said associated at least one switch output buffers.

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Add A⁴